WHAT IS CLAIMED IS:

1. An electrostatic discharge protection circuit device comprising:

a first electrostatic discharge protection circuit connected between a first external terminal supplied with a first power supply voltage at time of ordinary operation and a first ground terminal;

a second electrostatic discharge protection circuit connected between a second external terminal supplied with a second power supply voltage at the time of the ordinary operation and a second ground terminal, the second electrostatic discharge protection circuit having substantially the same configuration as that of the first electrostatic discharge protection circuit;

a trigger signal line which connects to each other output nodes of surge detection circuits of the first and second electrostatic discharge protection circuits, and transfers a surge detection output of one of the first and second electrostatic discharge protection circuits to the other electrostatic discharge protection circuit as a trigger signal; and

a common discharge line connected directly to the first ground terminal, connected to the second ground terminal via a parallel circuit composed of a forward-connected parasitic diode element and a reverse-connected parasitic diode element, and used commonly by the first and second of electrostatic discharge

protection circuits.

2. The electrostatic discharge protection circuit device according to claim 1, wherein each of the first electrostatic discharge protection circuit and the second electrostatic discharge protection circuit comprises a voltage clamp element, a trigger circuit, and a surge detection circuit.

3. The electrostatic discharge protection circuit device according to claim 2, wherein

the voltage clamp element comprises an SCR for ESD protection composed of a PNP transistor and an NPN transistor, the SCR being connected between the external terminal and ground terminal associated therewith respectively at an anode and a cathode of the SCR,

the trigger circuit comprises a first PMOS transistor for SCR trigger connected between the external terminal associated therewith and the base of the NPN transistor respectively at a source and a drain thereof, connected to a substrate region at the source thereof, and connected to a trigger bias line, and an NMOS transistor for SCR trigger connected between a base of the PNP transistor and the ground terminal associated therewith respectively at a drain and a source thereof, connected to a substrate region at the source thereof, and connected to the trigger signal line at a gate thereof, and

the surge detection circuit comprises a second PMOS transistor for surge detection inserted between the external terminal associated therewith and the trigger signal line and connected to a substrate region at the source thereof, and a diode connected in series with the second PMOS transistor in a forward direction.

4. The electrostatic discharge protection circuit device according to claim 2, further comprising a third electrostatic discharge protection circuit which includes a voltage clamp and trigger element, connected between a third external terminal for signal input/output electrically isolated from the first external terminal and the second ground terminal, and a second surge detection circuit, an output node of the second surge detection circuit being connected to the trigger signal line.

5. The electrostatic discharge protection circuit device according to claim 4, wherein

the voltage clamp and trigger element comprises an NMOS transistor connected between the third external terminal and the second ground terminal respectively at a drain and a source thereof, connected to a substrate region at the source thereof, and connected to the trigger signal line at a gate thereof, and

the second surge detection circuit comprises a second PMOS transistor for surge detection inserted between the third external terminal and the trigger

signal line and connected to a substrate region at the source thereof, and a diode connected in series with the second PMOS transistor in a forward direction.

6. The electrostatic discharge protection circuit device according to claim 1, further comprising:

an integration circuit connected between the first or second external terminal supplied with a highest potential of those potentials supplied to the first external terminal and the second external terminal and the ground terminal associated with the external terminal supplied with the highest potential, and

a trigger bias line connected in common to an output node of the integration circuit and to gates of surge detection elements and trigger elements in the first and second electrostatic discharge protection circuits.

7. The electrostatic discharge protection circuit device according to claim 1, further comprising a potential holding circuit connected to the trigger signal line to keep a potential on the trigger signal line at time when a power supply of the circuit device is turned on constant.

8. The electrostatic discharge protection circuit device according to claim 7, wherein the potential holding circuit comprises:

a capacitance element connected to the trigger signal line, which holds electric charges;

a resistor element which determines a time constant in cooperation with the capacitance element so as to prevent the trigger signal from being generated at the time when the power supply of the circuit device is turned on and discharges electric charges held by the capacitance element, the resistor element being connected to the trigger signal line; and

a voltage limiter element connected to the trigger signal line.

9. The electrostatic discharge protection circuit device according to claim 6, wherein each of the first and second electrostatic discharge protection circuits has a configuration in which each of the first and second electrostatic discharge protection circuits is set to a protection operation state by an external signal supplied from outside of a semiconductor integrated circuit device incorporating the first and second electrostatic discharge protection circuits.

10. The electrostatic discharge protection circuit device according to claim 6, wherein each of the first and second electrostatic discharge protection circuits has a configuration in which each of the first and second electrostatic discharge protection circuits is set to a protection operation state by setting a circuit in a semiconductor integrated circuit device incorporating the first and second electrostatic discharge protection circuits.

11. The electrostatic discharge protection circuit device according to claim 9, further comprising a fuse element connected between the trigger bias line and a ground terminal in the semiconductor integrated circuit device,

wherein the fuse element is blown out from the outside of the semiconductor integrated circuit device after the semiconductor integrated circuit device is mounted on a circuit board of an application product.

12. The electrostatic discharge protection circuit device according to claim 10, further comprising a switch element connected between the trigger bias line and a ground terminal in the semiconductor integrated circuit device,

wherein the switch element is controlled to be in an on-state until the semiconductor integrated circuit device is mounted on a circuit board of an application product, and the switch element is controlled to be in an off-state after the semiconductor integrated circuit device is mounted on the circuit board of the application product.

13. The electrostatic discharge protection circuit device according to claim 10, further comprising:

an external setting terminal connected to the trigger bias line; and

a pull-down resistor element between the external setting terminal and a ground line within the

semiconductor integrated circuit device,

wherein the external setting terminal is connected to a power supply wiring pattern on the circuit board when the semiconductor integrated circuit device has been mounted on a circuit board of an application product.

14. The electrostatic discharge protection circuit device according to claim 3, further comprising:

first and second NMOS transistors for DC trigger associated with and connected in parallel to the NMOS transistor for trigger included in the first electrostatic protection circuit and the NMOS transistor for trigger included in the second electrostatic protection circuit, respectively; and

a DC trigger line which transfers a base potential at an NPN transistor in the SCR in one of the first and second electrostatic protection circuits to a gate of the NMOS transistor for DC trigger in the other electrostatic protection circuit.

15. The electrostatic discharge protection circuit device according to claim 3, further comprising:

a third electrostatic discharge protection circuit which includes a voltage clamp and trigger element, connected between a third external terminal for signal input/output electrically isolated from the first external terminal and the second ground terminal, and a second surge detection circuit, an output node of the

second surge detection circuit being connected to the trigger signal line.

first and second NMOS transistors for DC trigger associated with and connected in parallel to the NMOS transistor for trigger included in the first electrostatic protection circuit and the NMOS transistor for trigger included in the second electrostatic protection circuit, respectively;

a third NMOS transistor for DC trigger associated with and connected in parallel to an NMOS transistor for voltage clamp and trigger included in the third electrostatic protection circuit; and

a DC trigger line which transfers a base potential at an NPN transistor in the SCR in one of the first, second and third electrostatic protection circuits to a gate of the NMOS transistor for DC trigger in the other electrostatic protection circuits.

16. An electrostatic discharge protection circuit device comprising:

a first electrostatic discharge protection circuit connected between a first external terminal supplied with a first power supply voltage at time of ordinary operation and a first ground terminal;

a plurality of second electrostatic discharge protection circuits each connected between a corresponding second external terminal supplied with a corresponding second power supply voltage at the time

of the ordinary operation and a corresponding second ground terminal, each of the second electrostatic discharge protection circuits having substantially the same configuration as that of the first electrostatic discharge protection circuit;

a trigger signal line which connects in common an output node of a surge detection circuit of the first electrostatic discharge protection circuit and output nodes of surge detection circuits of the second electrostatic discharge protection circuits, and transfers a surge detection output of the first electrostatic discharge protection circuit and a surge detection output of one of the second electrostatic discharge protection circuits to the other electrostatic discharge protection circuits as a trigger signal; and

a common discharge line connected directly to the first ground terminal, connected to the second ground terminals via a parallel circuit composed of a forward-connected parasitic diode element and a reverse-connected parasitic diode element, and used commonly by the first electrostatic discharge protection circuit and the second of electrostatic discharge protection circuits.

17. The electrostatic discharge protection circuit device according to claim 16, wherein the first electrostatic discharge protection circuit and each of

the second electrostatic discharge protection circuits comprise a voltage clamp element, a trigger circuit, and a surge detection circuit.

18. The electrostatic discharge protection circuit device according to claim 17, wherein

the voltage clamp element comprises an SCR for ESD protection composed of a PNP transistor and an NPN transistor, the SCR being connected between the external terminal to which the corresponding electrostatic discharge protection circuit is connected and the ground terminal associated therewith respectively at an anode and a cathode of the SCR,

the trigger circuit comprises a first PMOS transistor for SCR trigger connected between the external terminal to which the corresponding electrostatic discharge protection circuit is connected and the base of the NPN transistor respectively at a source and a drain thereof, connected to a substrate region at the source thereof, and connected to a trigger bias line, and an NMOS transistor for SCR trigger connected between a base of the PNP transistor and the ground terminal to which the corresponding electrostatic discharge protection circuit is connected respectively at a drain and a source thereof, connected to a substrate region at the source thereof, and connected to the trigger signal line at a gate thereof, and

the surge detection circuit comprises a second

PMOS transistor for surge detection inserted between the external terminal to which the corresponding electrostatic discharge protection circuit is connected and the trigger signal line and connected to a substrate region at the source thereof, and a diode connected in series with the second PMOS transistor in a forward direction.

19. The electrostatic discharge protection circuit device according to claim 17, further comprising a third electrostatic discharge protection circuit which includes a voltage clamp and trigger element, connected between a third external terminal for signal input/output electrically isolated from the first external terminal and one of the second ground terminals, and a second surge detection circuit, an output node of the second surge detection circuit being connected to the trigger signal line.

20. The electrostatic discharge protection circuit device according to claim 19, wherein

the voltage clamp and trigger element comprises an NMOS transistor connected between the third external terminal and the one of the second ground terminals respectively at a drain and a source thereof, connected to a substrate region at the source thereof, and connected to the trigger signal line at a gate thereof, and

the second surge detection circuit comprises a

second PMOS transistor for surge detection inserted between the third external terminal and the trigger signal line and connected to a substrate region at the source thereof, and a diode connected in series with the second PMOS transistor in a forward direction.

21. The electrostatic discharge protection circuit device according to claim 16, further comprising:

an integration circuit connected between the first external terminal or one of the second external terminals supplied with a highest potential of those potentials supplied to the first external terminal and the second external terminals, and the ground terminal associated with the external terminal supplied with the highest potential, and

a trigger bias line connected in common to an output node of the integration circuit and to gates of surge detection elements and trigger elements in the first electrostatic discharge protection circuit and the second electrostatic discharge protection circuits.

22. The electrostatic discharge protection circuit device according to claim 16, further comprising a potential holding circuit connected to the trigger signal line to keep a potential on the trigger signal line at time when a power supply of the circuit device is turned on constant.

23. The electrostatic discharge protection circuit device according to claim 22, wherein the potential

holding circuit comprises:

a capacitance element connected to the trigger signal line, which holds electric charges;

a resistor element which determines a time constant in cooperation with the capacitance element so as to prevent the trigger signal from being generated at the time when the power supply of the circuit device is turned on and discharges electric charges held by the capacitance element, the resistor element being connected to the trigger signal line; and

a voltage limiter element connected to the trigger signal line.

24. The electrostatic discharge protection circuit device according to claim 21, wherein the first electrostatic discharge protection circuit and each of the second electrostatic discharge protection circuits have a configuration in which the first electrostatic discharge protection circuit and each of the second electrostatic discharge protection circuits are set to a protection operation state by an external signal supplied from outside of a semiconductor integrated circuit device incorporating the first electrostatic discharge protection circuit and the second electrostatic discharge protection circuits.

25. The electrostatic discharge protection circuit device according to claim 21, wherein the first electrostatic discharge protection circuit and each of

the second electrostatic discharge protection circuits have a configuration in which the first electrostatic discharge protection circuit and each of the second electrostatic discharge protection circuits are set to a protection operation state by setting a circuit in a semiconductor integrated circuit device incorporating the first electrostatic discharge protection circuit and the second electrostatic discharge protection circuits.

26. The electrostatic discharge protection circuit device according to claim 24, further comprising a fuse element connected between the trigger bias line and a ground terminal in the semiconductor integrated circuit device,

wherein the fuse element is blown out from the outside of the semiconductor integrated circuit device after the semiconductor integrated circuit device is mounted on a circuit board of an application product.

27. The electrostatic discharge protection circuit device according to claim 25, further comprising a switch element connected between the trigger bias line and the one of the ground terminals in the semiconductor integrated circuit device,

wherein the switch element is controlled to be in an on-state until the semiconductor integrated circuit device is mounted on a circuit board of an application product, and the switch element is controlled to be in

an off-state after the semiconductor integrated circuit device is mounted on the circuit board of the application product.

28. The electrostatic discharge protection circuit device according to claim 25, further comprising:

an external setting terminal connected to the trigger bias line; and

a pull-down resistor element between the external setting terminal and a ground line within the semiconductor integrated circuit device,

wherein the external setting terminal is connected to a power supply wiring pattern on the circuit board when the semiconductor integrated circuit device has been mounted on a circuit board of an application product.

29. The electrostatic discharge protection circuit device according to claim 16, wherein

a plurality of electrostatic discharge protection circuits including the first electrostatic discharge protection circuit and the second electrostatic discharge protection circuits and having the substantially same configuration as that of the first electrostatic discharge protection circuit and each of the second electrostatic discharge protection circuits are formed in a semiconductor integrated circuit device, and

an output of a surge detection circuit of the

electrostatic discharge protection circuit among the plurality of electrostatic discharge protection circuits that has first detected that electrostatic charge has been applied is supplied to other electrostatic discharge protection circuits via the trigger signal line as a trigger input.

30. The electrostatic discharge protection circuit device according to claim 19, further comprising:

a plurality of NMOS transistors for DC trigger associated with and connected in parallel to the NMOS transistors for trigger included in the first electrostatic protection circuit and the second electrostatic protection circuits; and

a DC trigger line which transfers a base potential at the NPN transistor in the SCR in one of the electrostatic protection circuits to gates of the NMOS transistors for DC trigger in other electrostatic protection circuits.

31. The electrostatic discharge protection circuit device according to claim 19, further comprising:

a third electrostatic discharge protection circuit which includes a voltage clamp and trigger element, connected between a third external terminal for signal input/output electrically isolated from the first external terminal and one of the second ground terminals, and a second surge detection circuit, an output node of the second surge detection circuit being

connected to the trigger signal line.

a plurality of NMOS transistors for DC trigger associated with and connected in parallel to the NMOS transistors for trigger included in the first and second electrostatic protection circuits;

a NMOS transistor for voltage clamp and trigger included in the third electrostatic protection circuit; and

a DC trigger line which transfers a base potential at the NPN transistor in the SCR in the first electrostatic protection circuit and one of the second electrostatic protection circuits to gates of the NMOS transistors for DC trigger in other electrostatic protection circuits.